Claims

[c1] BUR920030070US1

1. A voltage regulated power supply test circuit comprising:

a voltage regulator electrically connected to at least one regulated voltage node of a functional circuit of an integrated circuit chip; and

a circuit capable of selectively connecting between one of said at least one regulated voltage nodes and ground with at least one load circuit adapted to put an emulated current load of said functional circuit on said regulated voltage supply.

[c2] 2. The circuit of claim 1, further including a reference voltage generator electrically connected between said voltage regulator and a power supply.

[c3] 3. The circuit of claim 2, wherein said power supply is external to said integrated circuit chip.

[c4] 4. The circuit of claim 1, wherein said load circuit comprises a gated resistive load.

[c5] 5 The circuit of claim 1, wherein said load circuit comprises a current mirror.

[c6] 6. The circuit of claim 5, further including means for varying the amount of current flowing through said load circuit.

[c7] 7. The circuit of claim 6, wherein said current mirror includes selectable multiple mirror elements each electrically connectable to different voltage sources having different on/off patterns.

[c8] 8. The circuit of claim 1, further including at least one test point, each said at least one test point electrically connected to one of said at least one regulated voltage nodes.

[c9] 9. The circuit of claim 8, wherein said one or more test points is an I/O monitor pad of said integrated circuit chip.

[c10] 10. The circuit of claim 1, further including:
multiple test points, each test point connected to a different regulated voltage node of said functional circuit; and
a circuit capable of combining the voltages on each test point into a signal on one or more I/O monitor pads, a number of said monitor pads being less than a number of said test points.

[c11] 11. The circuit of claim 10, wherein said circuit capable of combining the voltages includes:
a multiplicity of voltage comparators, a first input of each voltage comparator connected to a different test point, a second input of said voltage comparator connected to a voltage supply, an output of each said comparator connected to inputs of a compression logic and said one or more I/O monitor pads connected to outputs of said compression logic.

[c12] 12. The circuit of claim 10, wherein said circuit capable of combining the voltages includes:
a different test point connected to each input of a multiplexer and an output of said multiplexer connected to an analog to digital converter, said multiplexer and said analog to digital converter responsive to control signals from a control state machine, the output of said analog to digital converter connected to one or more of said I/O monitor pads.

[c13] 13. The circuit of claim 10, wherein said circuit capable of combining the voltages includes:
a different test point connected to each input of a multiplexer and an output of said multiplexer connected to an analog to digital converter, said multiplexer and said analog to digital converter responsive to control signals from a control state machine, the output of said analog

to digital converter connected to a compressed storage device, said compressed storage device responsive to said control signals, and said compressed storage device connected to said one or more of said I/O monitor pads.

[c14] 14. The circuit of claim 1, wherein:
said regulated voltage nodes are located on a regulated voltage grid;
said functional circuit includes component circuits, each component circuit connected between one said at least one regulated voltage node and a ground node on a ground grid having multiple ground nodes; and
each said at least one load circuit also connected to a ground node.

[c15] 15. The circuit of claim 14, further including additional voltage regulators, all said voltage regulators located around the periphery of said integrated circuit chip, each voltage regulator connected to different said one or more regulated voltage nodes.

[c16] 16. A method of testing a voltage regulated power supply comprising:
providing a voltage regulator electrically connected to at least one regulated voltage node of a functional circuit of an integrated circuit chip; and
selectively connecting between one of said at least one

regulated voltage nodes and ground at least one load circuit adapted to put an emulated current load of said functional circuit on said regulated voltage supply.

[c17] 17. The method of claim 16, further including providing a reference voltage generator electrically connected between said voltage regulator and a power supply.

[c18] 18. The method of claim 17, wherein said power supply is external to said integrated circuit chip.

[c19] 19. The method of claim 16, wherein said load circuit comprises a gated resistive load.

[c20] 20 The method of claim 16, wherein said load circuit comprises a current mirror.

[c21] 21. The method of claim 20, further including varying the amount of current flowing through said load circuit.

[c22] 22. The method of claim 21, wherein said current mirror includes selectable multiple mirror elements each having different on/off patterns voltage sources and further comprising selectively connecting one or more of said mirror elements to said load circuit.

[c23] 23. The method of claim 16, further including providing at least one test point, each said at least one test point electrically connected to one of said at least one regu-

lated voltage nodes.

[c24] 24. The method of claim 23, wherein said at least one test points is an I/O monitor pad of said integrated circuit chip.

[c25] 25. The method of claim 16, further including:
providing multiple test points, each test point connected to a different regulated voltage node of said functional circuit; and
combining the voltages on each test point into a signal on one or more I/O monitor pads, a number of said monitor pads being less than a number of said test points.

[c26] 26. The method of claim 25, wherein the step of combining includes:
providing a multiplicity of voltage comparators, a first input of each voltage comparator connected to a different test point, a second input of said voltage comparator connected to a voltage supply, an output of each said comparator connected to inputs of a compression logic and said one or more I/O monitor pads connected to outputs of said compression logic.

[c27] 27. The method of claim 25, wherein the step of combining includes:

providing a multiplexer, a different test point connected to each input of said multiplexer, an output of said multiplexer connected to an analog to digital converter, said multiplexer and said analog to digital converter responsive to control signals from a control state machine, and the output of said analog to digital converter connected to one or more of said I/O monitor pads.

[c28] 28. The method of claim 25, wherein the step of combining includes:
providing a multiplexer, a different test point connected to each input of said multiplexer, an output of said multiplexer connected to an analog to digital converter, said multiplexer and said analog to digital converter responsive to control signals from a control state machine, the output of said analog to digital converter connected to a compressed storage device, said compressed storage device responsive to said control signals, and said compressed storage device connected to said one or more of said I/O monitor pads.

[c29] 29. The method of claim 16, wherein;
said regulated voltage nodes are located on a regulated voltage grid;
said functional circuit includes component circuits, each component circuit connected between one said at least one regulated voltage node and a ground node on a

ground grid having multiple ground nodes; and
each said at least one load circuit also connected to a ground node.

[c30] 30. The method of claim 29, further including providing additional voltage regulators, all said voltage regulators located around the periphery of said integrated circuit chip, each voltage regulator connected to different said one or more regulated voltage nodes.